



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,076	08/22/2003	John S. Montrym	NVID-P000705	9603

7590 04/19/2006  
WAGNER, MURABITO & HAO LLP  
Third Floor  
Two North Market Street  
San Jose, CA 95113

EXAMINER

HSU, JONI

ART UNIT PAPER NUMBER

2628

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/646,076	Applicant(s) MONTRYM ET AL.	
	Examiner Joni Hsu	Art Unit 2628	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 03 February 2006.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-25 and 27-44 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25, 27-36 and 38-42 is/are rejected.
- 7) ☒ Claim(s) 37, 43 and 44 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. Applicant's arguments with respect to claims 1-25 and 27-36, and 38-42 have been considered but are moot in view of the new ground(s) of rejection.
2. Applicant's arguments, see pages 13-25, filed February 3, 2006, with respect to the rejection(s) of claim(s) 28-32 and 35 under 35 U.S.C. 102(e) and claims 1-25, 27-36, and 38-42 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Morein (US006188394B1).
3. Applicant argues that Vugt (US006833835B1) teaches that hi-resolution pixels are not put in memory. As such, since addresses point to locations in memory, Vugt teaches that addresses to high-resolution pixels do not exist, and therefore fails to teach a subpixel address (page 14).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Morein.

4. Applicant's arguments, see pages 23-25, filed February 3, 2006, with respect to Claims 37, 43, and 44 have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejections of Claims 37, 43, and 44 has been withdrawn.

*Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Morein (US006188394B1).

7. With regard to Claim 28, Morein describes a method for reading a frame buffer (36, Figure 2; *primary memory is frame buffer*, Col. 3, lines 19-23; *data is retrieved from primary memory*, Col. 4, lines 9-13), the method comprising receiving an address corresponding to a pixel (*pointer is stored at the frame buffer location corresponding to the particular pixel*, Col. 2, lines 18-20); transforming the received address into at least one subpixel (sample) address (*pointer points to a selected address in a sample memory at which the complete sample set for the pixel is stored*, Col. 2, lines 20-23; *each pixel is described by a number of samples*, Col. 2, lines 25-31); reading at least one subpixel from the frame buffer using at least one subpixel address (*data is retrieved by the pointer stored in the frame buffer*, Col. 4, lines 9-13), wherein the frame buffer is a single memory comprising a plurality of pixels (Col. 3, lines 19-22), wherein each pixel comprises a plurality of subpixels (Col. 2, lines 25-31); and blending the at

least one subpixel to create a pixel value (*samples are combined to produce a resultant color value for the particular pixel*, Col. 2, lines 25-31).

8. With regard to Claim 29, Claim 29 is similar in scope to Claim 28, except that Claim 29 has the extra step of supplying the created pixel value. Morein describes supplying the created pixel value as if it were a pixel value at the received address (Col. 4, lines 6-14). Therefore, Claim 29 is rejected under the same rationale as Claim 28.

9. With regard to Claim 30, Morein describes a method for writing a frame buffer (36, Figure 2) comprising receiving an address and a pixel value from a computer program (84, Figure 4; Col. 2, lines 19-21; *instructions 84 which cause the controller 82 to perform a predetermined function, the instructions 84 may be a software algorithm, receiving a pixel fragment*, Col. 8, lines 15-27), the computer program supplying the address and pixel value as if accessing a frame buffer that does not comprise subpixels; transforming the received address into at least one subpixel address; writing the pixel value to a frame buffer as at least two subpixel values using the at least one subpixel address (Col. 2, lines 19-23, 25-31) wherein the frame buffer is a single memory comprising a plurality of pixels (Col. 3, lines 6-20) wherein each pixel comprises a plurality of subpixels (Col. 5, lines 39-44).

10. With regard to Claim 31, Claim 31 is similar in scope to Claim 29, except Claim 31 supplies the read subpixel value. Morein describes supplying the read subpixel value as if it

were a pixel value at the received address (Col. 4, lines 9-14; Col. 2, lines 25-31). Therefore, Claim 31 is rejected under the same rationale as Claim 29.

11. Thus, it reasonably appears that Morein describes or discloses every element of Claims 28-31 and therefore anticipates the claims subject.

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 1-4, 9, 10, 13, 15-17, 19, 21-23, and 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein (US006188394B1) in view of Sturges (US005854637A).

15. With regard to Claim 1, Morein describes a method for providing antialiased memory access (Col. 2, lines 46-47; Col. 4, lines 9-13), comprising receiving a request to access a memory address (Col. 4, lines 9-13); and transforming the memory address into at least one physical address within a frame buffer (36, Figure 2) utilized for antialiasing (Col. 2, lines 19-23), wherein the frame buffer is a single memory for containing data of a plurality of subpixels corresponding to a pixel of the sample memory (Col. 2, lines 19-23, 25-31); and accessing data of a subpixel at the at least one physical address within the frame buffer (Col. 4, lines 9-13).

However, Morein does not teach that the sample memory is a virtual frame buffer and determining if the memory address is within a virtual frame buffer and, if so, performing the transforming and accessing. However, Sturges describes that if the address is within a virtual frame buffer, the address is transformed (*access to the frame buffer portion of the memory by the microprocessor or other client devices is provided through a virtual frame buffer device (VFBD) which recognizes the frame buffer portion of memory*, Col. 3, lines 28-32, *once an application program requires access to a frame buffer, the VFBD controls the VMM to set up paging tables for the frame buffer portion of the shared memory*, Col. 3, lines 62-65; *the frame buffer is defined within the second portion of memory*, Col. 4, lines 43-51; *VMM 50 defines a set of tables 56 relating physical address up to top of system memory 23 to virtual addresses*, Col. 8, lines 15-44).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Morein to include a virtual frame buffer as suggested by Sturges because Sturges suggests that this expedites graphics operations by allowing both the

graphics controller and the memory controller to write graphics data into the frame buffer (Col. 1, lines 23-34, 49-52; Col. 3, lines 7-10).

16. With regard to Claim 2, Morein does not teach accessing data at the memory address provided the memory address is not within the virtual frame buffer. However, Sturges describes accessing data at the memory address provided the memory address is not within the virtual frame buffer (Col. 3, lines 28-32, 62-65; *memory controller may freely access the system memory contained within the first portion of the physical memory at all times*, Col. 4, lines 43-56; Col. 8, lines 15-44). This would be obvious for the same reasons given in the rejection for Claim 1.

17. With regard to Claim 3, Morein does not teach describes that the virtual frame buffer comprises a predefined memory range of a graphics memory. However, Sturges describes that the virtual frame buffer comprises a predefined memory range of a graphics memory (*frame buffer is defined within the second portion of memory*, Col. 4, lines 40-60; *notify VMM 50 that the top of system memory is memory address 23 which is just below memory devoted to the frame buffer, pages are registered by the VMM for use by the VFBD, the pages are allocated for the exclusive use of the VFBD*, Col. 8, lines 14-21). This would be obvious for the same reasons given in the rejection for Claim 1.

18. With regard to Claim 4, Morein describes that the memory address is received from a central processing unit (CPU) (82, Figure 4; Col. 8, lines 43-45).



19. With regard to Claim 9, Claim 9 is similar to Claim 1, except that Claim 9 is for accessing data in order to read data. Morein describes accessing data in order to read data (Col. 4, lines 9-13). Therefore, Claim 9 is rejected under the same rationale as Claim 1.

20. With regard to Claim 10, Morein describes providing the subpixel value to a central processing unit (CPU) (82, Figure 4; Col. 8, lines 43-52).

21. With regard to Claim 13, Claim 13 is similar in scope to Claim 3, and therefore is rejected under the same rationale.

22. With regard to Claim 15, Claim 15 is similar in scope to Claim 9, except Claim 15 is for reading the plurality of subpixel values and combining the subpixel values. Morein describes reading the plurality of subpixel values at the plurality of physical addresses within the frame buffer (36, Figure 2; Col. 4, lines 9-13) and combining the subpixel values to generate a pixel value for the specific pixel (Col. 2, lines 25-31). Therefore, Claim 15 is rejected under the same rationale as Claim 9.

23. With regard to Claim 16, Morein describes providing the pixel value to a central processing unit (CPU) (82, Figure 4; Col. 8, lines 21-25).

24. With regard to Claim 17, Morein describes that the combining comprises blending the subpixel values into a single color value (Col. 2, lines 25-31).

25. With regard to Claim 19, Claim 19 is similar in scope to Claim 3, and therefore is rejected under the same rationale.

26. With regard to Claim 21, Claim 21 is similar to Claim 1, except that Claim 21 is for accessing data in order to write data. Morein describes accessing data in order to write data (Col. 2, lines 15-19). Therefore, Claim 21 is rejected under the same rationale as Claim 1.

27. With regard to Claim 22, Claim 22 is similar in scope to Claim 2, and therefore is rejected under the same rationale.

28. With regard to Claim 23, Morein does not teach that the virtual memory buffer includes a predefined memory range of graphics memory. However, Sturges describes that the virtual memory buffer comprises a predefined memory range of a graphics memory (Col. 4, lines 40-60; Col. 8, lines 14-21). This would be obvious for the same reasons given in the rejection for Claim 1.

29. With regard to Claim 32, Morein describes receiving an address in the sample memory from the computer program (Col. 5, lines 39-48; Col. 9, line 64-Col. 10, line 20); transforming the received address into at least one subpixel address (Col. 5, lines 39-48; Col. 5, line 59-Col. 6,

line 2), the subpixel address being an address into a frame buffer which is a single memory storing data of a plurality of subpixels corresponding to each pixel of the sample memory (Col. 2, lines 19-23, 25-31); reading at least two subpixels from the frame buffer using the subpixel address (Col. 4, lines 9-14); blending the at least two subpixels to create a pixel value (Col. 2, lines 25-31); supplying the created pixel value to the computer program as if it were a pixel value located at the received address in the sample; and wherein the computer program does not directly access the frame buffer (Col. 4, lines 9-14).

However, Morein does not teach that the sample memory is a virtual frame buffer, and supplying a base address and buffer size information corresponding to a virtual frame buffer. However, Sturges describes a method for supplying a virtual frame buffer to a computer program (Col. 3, lines 28-35), comprising supplying a base address and buffer size information to the computer program, the base address and the buffer size information corresponding to a virtual frame buffer (*notify VMM 50 that the top of system memory is memory address 23 which is just below memory devoted to the frame buffer*, Col. 8, lines 15-22, *VFBD queries the BIOS frame buffer unit 56 to determine the size of frame buffer 20*, Col. 8, lines 30-31); receiving an address in the virtual frame buffer from the computer program; transforming the received address into at least one address into a frame buffer which is a single memory storing data corresponding to the data of the virtual frame buffer; supplying the pixel value to the computer program as if it were a pixel value located at the received address in the virtual frame buffer; and wherein the computer program does not directly access the frame buffer (Col. 8, lines 15-44).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Morein to include supplying a base address and buffer size

information corresponding to a virtual frame buffer as suggested by Sturges because Sturges suggests that this enables the system to modify the size of the portion of memory devoted to the frame buffer (Col. 1, lines 55-58). The advantages of using a virtual frame buffer were discussed in the rejection for Claim 1.

30. With regard to Claim 33, Morein does not teach that the computer program is an operating system. However, Sturges describes that the computer program is an operating system (*BIOS transmits a signal to an operating system of the microprocessor identifying the top of system memory as being the bottom of the frame buffer portion of memory*, Col. 3, lines 23-26).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Morein so that the computer program is an operating system as suggested by Sturges because Sturges suggests that it is well-known in the art to use operating system software to perform operations on memory (Col. 1, lines 23-24; Col. 2, lines 2-5).

31. With regard to Claim 34, Morein does not teach that the computer program is a software driver. However, Sturges describes that the computer program is a software driver (client software (*ie., graphics device drivers*) request access to the frame buffer through the VFBD provider, Col. 9, lines 24-27).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Morein so that the computer program is a software driver as suggested by Sturges because Sturges suggests that a software driver is needed in order for a

client to request access to the frame buffer through the virtual frame buffer device (Col. 9, lines 24-27).

32. With regard to Claim 35, Morein describes that the computer program (84, Figure 4) is an application program (Col. 8, lines 16-21).

33. Claims 5, 6, 11, 12, 18, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein (US006188394B1) and Sturges (US005854637A) in view of Dye (US005664162A).

34. With regard to Claim 5, Morein and Sturges are relied upon for the teachings as discussed above relative to Claim 4.

However, Morein and Sturges do not teach providing the CPU with a pitch value of the frame buffer. However, Dye describes providing the CPU (128, Figure 1) with a pitch value of the frame buffer (110) (*CPU 128 controls the system bus 102 for providing data and instructions, host CPU 128 asserts address signals*, Col. 7, lines 59-66; *host data bus transfers data and instructions to and from the host computer system, which includes the host CPU 128*, Col. 9, lines 59-64; *pitch of the frame buffer 110*, Col. 12, lines 10-17).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Morein and Sturges to include providing the CPU with a pitch value of the frame buffer as suggested by Dye because Dye suggests that the CPU needs to know

the pitch value of the frame buffer in order to read data from the correct location corresponding with the virtual frame buffer (116) (Col. 3, lines 49-51; Col. 12, lines 1-24).

35. With regard to Claim 6, Morein and Sturges do not teach the CPU calculating a physical address within the frame buffer using the pitch value of the frame buffer as the pitch of the virtual frame buffer. However, Dye describes the CPU (128, Figure 1) calculating a physical address within the frame buffer (110) using the pitch value of the frame buffer as the pitch of the virtual frame buffer (116) (*private memory is virtual frame buffer*, Col. 3, lines 49-51; Col. 12, lines 1-24). This would be obvious for the same reasons given in the rejection for Claim 5.

36. With regard to Claim 11, Claim 11 is similar in scope to Claim 5, and therefore is rejected under the same rationale.

37. With regard to Claim 12, Claim 12 is similar in scope to Claim 6, and therefore is rejected under the same rationale.

38. With regard to Claim 18, Claim 18 is similar in scope to Claim 6, and therefore is rejected under the same rationale.

39. With regard to Claim 25, Claim 25 is similar in scope to Claim 18, and therefore is rejected under the same rationale.

40. Claims 7, 8, 14, 20, 27, and 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein (US006188394B1) and Sturges (US005854637A) in view of Baldwin (US005594854A).

41. With regard to Claim 7, Morein and Sturges are relied upon for the teachings as discussed above relative to Claim 1.

However, Morein and Sturges do not teach that the plurality of subpixels corresponding to the pixel of the virtual frame buffer have physical addresses that are nearby each other. However, Baldwin describes that the buffer must reside at contiguous physical addresses, and if the virtual memory buffer maps to non-contiguous physical memory, then the buffer must be divided into sets of contiguous physical memory pages (Col. 18, lines 45-52). Therefore, the plurality of subpixels (Col. 34, lines 61-67) corresponding to the pixel of the virtual frame buffer have physical addresses are nearby each other (Col. 18, lines 35-52).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Morein and Sturges so that the plurality of subpixels corresponding to the pixel of the virtual frame buffer have physical addresses that are nearby each other as suggested by Baldwin because Baldwin suggests that this is needed because the data in the physical memory needs to be transferred together (Col. 18, lines 35-52).

42. With regard to Claim 8, Morein does not teach that the physical addresses are also based on a base physical address which corresponds to the memory address. However, Sturges describes that the physical addresses are also based on a base physical address which

corresponds to the memory address (*notify VMM 50 that the top of system memory is memory address 23 which is just below memory devoted to the frame buffer*, Col. 8, lines 14-22).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Morein so that the physical addresses are also based on a base physical address which corresponds to the memory address as suggested by Sturges because Sturges suggests that a base addresses is needed to determine when the where the address range of the frame buffer starts in order to make sure that the physical addresses are in the address range of the frame buffer (Col. 8, lines 14-22).

43. With regard to Claim 14, Claim 14 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

44. With regard to Claim 20, Claim 20 is similar in scope to Claim 14, and therefore is rejected under the same rationale.

45. With regard to Claim 27, Claim 27 is similar in scope to Claim 20, and therefore is rejected under the same rationale.

46. With regard to Claim 38, Claim 38 is similar in scope to Claim 7, and therefore is rejected under the same rationale.



47. With regard to Claim 39, Claim 39 is similar in scope to Claim 32 except that Claim 39 is for writing the pixel value and the plurality of subpixels comprise nearby physical addresses. Morein describes writing the pixel value (Col. 2, lines 15-19).

However, Morein does not teach that the plurality of subpixels comprise nearby physical addresses. However, Baldwin describes that the buffer must reside at contiguous physical addresses, and if the virtual memory buffer maps to non-contiguous physical memory, then the buffer must be divided into sets of contiguous physical memory pages (Col. 18, lines 45-52). Therefore, the plurality of subpixels (Col. 34, lines 61-67) corresponding to the pixel of the virtual frame buffer have physical addresses are nearby each other (Col. 18, lines 35-52), as discussed in the rejection for Claim 7.

48. With regard to Claim 40, Morein does not teach that the computer program is an operating system. However, Baldwin describes that the computer program is an operating system (Col. 4, lines 40-44). This would be obvious for the same reasons given in the rejection for Claim 33.

49. With regard to Claim 41, Morein does not teach that the computer program is a software driver. However, Baldwin describes that the computer program is a software driver (Col. 26, lines 11-13). This would be obvious for the same reasons given in the rejection for Claim 34.

50. With regard to Claim 42, Claim 42 is similar in scope to Claim 35, and therefore is rejected under the same rationale.

51. Claims 24 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein (US006188394B1) and Sturges (US005854637A) in view of Priem (US005623692A).

52. With regard to Claim 24, Morein and Sturges are relied upon for the teachings as discussed above relative to Claim 23.

However, Morein and Sturges do not teach that a base address of the predefined memory range is the same as a base address of the frame buffer. However, Priem describes that a base address of the predefined memory range is the same as a base address of the frame buffer (*generate physical addresses starting from the virtual start address*, Col. 27, lines 24-29).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Morein and Sturges so that a base address of the predefined memory range is the same as a base address of the frame buffer as suggested by Priem because Priem suggests that in the case where an application program transfers commands requesting DMA operations directly to the input/out control unit 29 without operating system intervention, the application program has no knowledge of the physical addresses involved, so the base address of the predefined memory range is set to be the same as the base address of the frame buffer (Col. 27, lines 12-29).

53. With regard to Claim 36, Claim 36 is similar in scope to Claim 23, and therefore is rejected under the same rationale.

*Allowable Subject Matter*

54. Claims 37, 43, and 44 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

55. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken singly or in combination do not teach or suggest a method comprising transforming a received address into at least one subpixel address, the subpixel address being an address into a frame buffer which is a single memory storing data of a plurality of subpixels corresponding to each pixel of a virtual frame buffer; wherein the base address of the virtual frame buffer is the same as a base address of the frame buffer; further comprising supplying a pitch corresponding to the virtual frame buffer and being equal to a pitch of the frame buffer, as recited in Claims 37 and 44.

The prior art also does not teach a method comprising transforming a received address into at least one subpixel address, the subpixel address being an address into a frame buffer which is a single memory storing data of a plurality of subpixels corresponding to each pixel of a virtual frame buffer and wherein the plurality of subpixels comprise nearby physical addresses; wherein the base address of the virtual frame buffer is the same as a base address of the frame buffer, as recited in Claim 43.

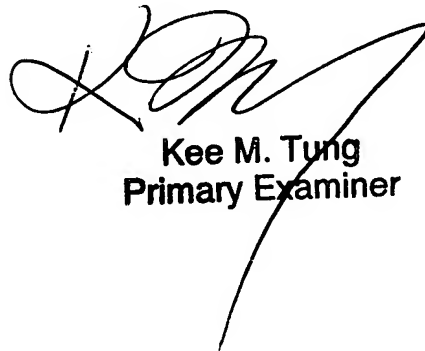
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH



**Kee M. Tung**  
**Primary Examiner**